REMARKS

In response to the Office Action dated February 6, 2008, claims 1, 11, 22, and 23 are amended, and claims 24-29 are cancelled without prejudice. Claims 1-23 remain in the application for consideration. No new matter has been added.

Claims11 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 1-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Trimberger in view of Official Notice of "branch units pushing return addresses on a stack-based register file." The Official Notice is provided at page 7 of the Office Action. This rejection is traversed. Applicants submit that this rejection is moot with respect to cancelled claims 24-28.

Independent claim 1 recites, in part, "a dedicated data processing facility having its own data register file, the data processing facility comprising a first data execution path including fixed operators and a second data execution path including at least configurable operators, said **configurable operators having a plurality of predefined hardwired operator classes, at least some of the interconnectivity of said operators is selectable by means of an opcode portion of a data processing instruction**; wherein said decode unit is operable to detect whether a data processing instruction defines a fixed data processing operation or a configurable data processing operation, said decode unit causing the computer system to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected." (Emphasis added)

FIG. 3 is an illustrative and non-limiting example of claim 1. The specification, at page 12, line 22 to page 13, line 2, states:

> In accordance with the embodiment of FIG. 3, the **operators are advantageously pre-configured into various operator classes. In practice, this is achieved by a strategic level of hardwiring.** An advantage of this approach is that it means that fewer predefined configurations need be stored, and that control circuitry can be simpler. **For example, operators 318 are pre-configured to be in the class of multiply operators;** operators 319 are pre-configured as ALU operators; operators 320 are preconfigured as state operators; and operators 321 are pre-configured as cross-lane permuters; and other pre-configured classes are possible. However, even though the classes of operators are pre-configured, there is nm-time flexibility for **instructions to be able to arrange at least: (i) connectivity of the operators within each class; (ii) connectivity with operators from the other classes; (ii) connectivity of any relevant switching means**; for the final arrangement of a specific configuration for implementing a given algorithm. (Emphasis added)

In other words, claim 1 uses an opcode portion of an instruction to select interconnectivity of predefined hardwired operators. **Thus, the predefined hardwired operators serve as building blocks for any new configuration, and greatly reduce the amount of reprogramming required to create a new configuration.**

Similar to independent claim 1, independent claim 22 states, "computer processor comprising a decode unit for decoding instructions, a dedicated control processing facility comprising a control execution path having its own control register file, and a dedicated data processing facility having its own data register file, the data processing facility comprising a first data execution path including fixed operators and a second data execution path including at least configurable operators, said **configurable operators having a plurality of predefined hardwired operator classes, at least some of the interconnectivity of said operators is selectable by means of an opcode portion of a data processing instruction.**" (Emphasis added)

Also similar to independent claim 1, independent claim 23 states: "computer processor comprising a decode unit for decoding instructions, a dedicated control processing facility comprising a control execution path having its own control register file, and a dedicated data processing facility having its own data register file, the data processing facility comprising a first data execution path including fixed operators and a second data execution path including at least configurable operators, said **configurable operators having a plurality of predefined hardware operator classes, at least some of the interconnectivity of said operators is selectable by means of an opcode portion of a data processing instruction**." (Emphasis added)

As is well known, anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987). The elements must be arranged as required by the claim. *In re Bond*, 910 F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitation.

The Office Action, at page 4 and page 7, asserts that Trimberger, at FIG. 2, item 120, discloses configurable operators having a plurality of predefined configurations. However, item 120 in FIG. 2 of Trimberger is field programmable gate array. Specifically, Trimberger, at column 7, line 57 to column 8, line 50, states:

> According to the present invention, a **reprogrammable instruction set accelerator** is included on the chip. Thus, a **RISA field programmable gate array (RISA FPGA) 120** is coupled to the internal buses 101 and 102, to receive operand data at ports A and B and supply result data at port Y to and from the buses. The opcode from line 114 is supplied at an instruction port I on the RISA FPGA 120. Condition codes generated by the RISA FPGA 120 are supplied on line 121 to the condition code register 108. These condition codes may use the same spaces in the condition code register 108 as the defined execution unit 100,

> use separate bits within the same register 108, or use a different register altogether coupled to operate in parallel with the condition code register 108 for the defined instructions. . .
>
> The signal on the configuration done port CD is used by the RISA FPGA 120 to delineate a configuration process in the RISA FPGA 120. This port is coupled to the condition code register or the instruction control state machine as necessary, as indicated by line 126. The configuration done signal is used during **reconfiguration of the RISA FPGA.** In one state, the system is held while the RISA FPGA loads configuration data. The other state, the system is signaled that the RISA FPGA is ready for execution. This system may be configured such that **during reconfiguration of the RISA FPGA 120, the defined execution unit 100 is capable of continuing execution as long as an opcode for the RISA is not encountered.** Alternatively, the system may be held up completely to allow for reconfiguration of the RISA FPGA 120. (Emphasis added)

Please note that RISA stands for Reduced Instruction Set Architecture, and FPGA stands for Field Programmable Gate Array. Thus, element 120 in FIG. 3 of Trimberger is merely a field programmable gate array which has been programmed into a processor configured to execute instructions based on a reduced instruction set.

The Office Action, at page 7, also cites Trimberger at column 2, line 62 to column 3, line 9, which states:

> The present invention provides a technique providing a reprogrammable instruction set accelerator (RISA). The RISA can be programmed with reprogrammable logic to do small scale data manipulation and computation, just like the instruction set accelerators currently in use. Furthermore, **the RISA can be tightly coupled to instruction and data paths in parallel with the predefined execution units in microprocessors.** This provides fast and efficient execution of new instructions and a significant improvement in performance. The RISA provides the capability for users to program instructions that may be difficult to do in the general purpose processor, and **not in wide enough use to warrant a hardware accelerator**. Further, the reprogrammable instruction set accelerator can be reprogrammed with different instructions at different times, saving space and cost in the computer. (Emphasis added)

The term "predefined execution units in microprocessors" in Trimberger appears to be used to refer to non-programmable (non-FPGA) microprocessors such as element 100 (EXEC

UNIT) in FIG. 2 of Trimberger. In other words, the RISA FPGA 120 of FIG. 2 may be programmed to interact with non-programmable microprocessors such as element 100.

In contrast to claim 1, Trimberger merely discloses "reconfiguring" the RISA FPGA at column 8, line 41. Trimberger does teach or suggest predefined hardwired operator classes, and does not teach or suggest that interconnectivity of said operators is selectable by means of an opcode portion, as required by claim 1.

Further, please note that the Trimberger discussion of opcodes is limited to allowing reconfiguration of the RISA FPGA, "as long as the opcode for the RISA is not encountered," as stated at column 8, lines 45-48.

Thus, Trimberger does not teach or suggest "configurable operators having a plurality of **predefined hardwired operator classes**, at least some of the **interconnectivity of said operators is selectable by means of an opcode portion** of a data processing instruction," as recited by claim 1. (Emphasis added)

Additionally, the Official Notice does not remedy the deficiencies of Trimberger. Further, Applicants traverse the Official Notice that "branch units pushing return addresses on a stack-based register file." However, to set forth a rejection including Official Notice, the rejection must include some form of evidence in the record to support an assertion of common knowledge. If Official Notice is taken of a fact, unsupported by documentary evidence, then the basis for such reasoning must be set forth explicitly. The Examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge. *See,* MPEP 2144.03(B). It is well settled that "the Board [and the Examiner] cannot simply reach conclusions based on [their] own understanding or experience - or on [their] assessment of what would be basic knowledge or common sense. Rather the Board

[and the Examiner] must point to some concrete evidence in the record in support of these findings." *In re Zurko*, 258 F. 3d 1379, 1386 (Fed. Cir. 2001). *See also, In re Lee*, 277 F. 3d 1338, 1344-45 (Fed. Cir. 2002), in which the court required evidence for the determination of unpatentability by clarifying that the principles of "*common knowledge*" and "*common sense*" may only be applied to the analysis of evidence, rather than be a substitute for evidence. Contrary to these requirements, the outstanding Office Action provides no sound technical and scientific reasoning to support the above recited Official Notice. The relied upon motion must be evidenced in the record, and cannot be based merely on an opinion of the Examiner.

Thus, at a minimum, the combination of Trimberger and Official Notice fails to teach or suggest the forgoing limitation, and therefore claim 1 is allowable over the cited art.

Referring to Ko, in order to create a circuit having a specific function, a typical wafer is provided with an arrangement of transistors connected using conductive wiring lines. The specific arrangement of transistors and wiring line sets the function of the circuit. Therefore, the circuit is created for the specific function at manufacture.

A gate array comprises a plurality of transistors provided in a pre-set regular pattern on a wafer. Then for each of a plurality of different functions, different wiring patterns can be applied to the wafer, such that a plurality of wafers having the same pre-set transistor layout, but with different wiring arrangements connecting the transistors, and thus different functions results. Again, the wiring pattern and thus function of the circuit is set at manufacture. The gate array is not programmable, so following manufacture, the function of the circuit cannot be changed.

A field programmable gate array (FPGA) can be programmed to change its function following manufacture. A FPGA comprises a plurality of logic gates connected together by wire

and a lot of switches. Each switch is controlled by a memory cell . Altering which switches are open or closed result in changing the function of the FPGA.

Ko discloses a gate array, i.e. a circuit whose function is set at manufacture, NOT a FPGA. For example, Ko at column 4, lines 31 to 33, states that "*the entirety of the user-definable circuitry area could be manufactured as a gate array*" and Ko at column 4, line 48 states that "*the fabrication process is completed by forming addition layers of metal and contacts on the surface of the user-definable circuitry area*". Furthermore, Ko at column 5, lines 13 to 14, recites that "*the circuits necessary for a specific application are chosen prior to fabrication*" - and thus are NOT programmable, and Ko at column 5, lines 19 to 21 states that "*for a specific application, the specific circuits are chosen from this library of potential circuits*".

Therefore, it is clear from the entirety of Ko's disclosure that the circuits function is set at manufacture and is not programmable.

The Examiner appears to believe that Ko discloses a FPGA. However, as stated above, the circuit of Ko is only definable at manufacture, it is not controllable by a processor. The running of software does not change the function of the gate array of Ko. In contrast the present application discloses circuitry which is definable under the control of software.

The Examiner specifically refers to figure 2 of Ko. However, figure 2 of Ko illustrates switches which are controlled by a test mode signal, which tests the internal circuit. The test signal comes from the test pin, not from a processor. Ko does not show a configurable interconnection of hardware.

Referring again to Trimberger, the latter appears to be the closest prior art, as asserted by the Examiner. However, Trimberger does not disclose (as admitted by the Examiner), at least, "*a dedicated control processing facility*", a dedicated data execution path including "*at least*

configurable operators and a controller, said configurable operators pre-configured into a plurality of hardwired operator classes" or the controller being "*operable to configure the connectivity of said configurable operators in accordance with configuration information provided in an opcode portion of said configurable data processing instruction*", as claimed in the independent claims of the present application Ko does not add anything to the teachings of Trimberger as it relates to gate arrays, not programmable arrays.

Therefore, any combination of the teachings of Trimberger and Ko would not result in the subject matter of the independent claims of the present application. Thus, the claims of the present application are novel and provide an inventive step over Trimberger, Ko and any combination of Trimberger and Ko.

Applicants respectfully submit that independent claims 22 and 23 are allowable, at a minimum, for the same reasons as independent claim 1.

Under Federal Circuit guidelines, a dependent claim is allowable if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819 F.2d at 1100, 1108 (Fed. Cir. 1987).

Thus, as independent claim 1 is allowable for the reasons set forth above, it is respectfully submitted that dependent claims 2-21 are allowable for at least the same reasons.

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

This amendment is being filed with a Request for Continued Prosecution, an Information Disclosure Statement, a Petition for an Extension of Time under 37 C.F.R. 1.136, and PTO Form SB/84 - Authorization to Act In A Representative Capacity. Please credit any overpayment or charge any shortage in fees due in connection with the filing of this paper, including fees associated with the Request for Continued Prosecution, the Information Disclosure Statement, and the Petition for an Extension of Time to Deposit Account 50-1133.

Respectfully submitted,

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